

● General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

● Features

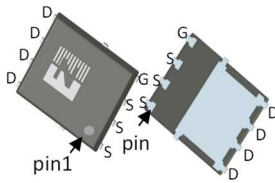
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low thermal resistance
- AEC-Q101 qualified

● Application

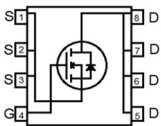
- BLDC motor driver
- DC-DC
- Battery protection



● Product Summary



DFN5*6



$V_{DS}=40V$

$R_{DS(ON)}=1m\Omega$

$I_D=243A$



● Ordering Information

Part NO.	ZMSA010N04HNC
Marking	ZMS010N04H
Packing information	REEL TAPE
Basic ordering unit (pcs)	3000

● Absolute Maximum Ratings ($T_A=25^\circ C$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Drain-source voltage	V_{DS}		-	40	V
Gate-source voltage ^①	V_{GS}		-20	20	V
Continuous drain current	I_D	$V_{GS}=10V, T_C=25^\circ C$	-	243	A
	I_D	$V_{GS}=10V, T_C=75^\circ C$	-	198	A
	I_D	$V_{GS}=10V, T_C=100^\circ C$	-	172	A
Pulsed drain current ^①	I_{DM}	Pulsed; $t_p \leq 10 \mu s; T_C = 25^\circ C$;	-	729	A
Diode continuous current	I_S	$V_{GS}=0V, T_C=25^\circ C$	-	96	A
Diode pulse current	$I_{S,pulse}$	Pulsed; $t_p \leq 10 \mu s; T_C = 25^\circ C$;	-	288	A
Total power dissipation	P_D	$T_C=25^\circ C$	-	125	W
Total power dissipation	P_D	$T_A=25^\circ C$	-	5	W
Operating junction temperature	T_J		-55	175	$^\circ C$
Storage temperature	T_{STG}		-55	175	$^\circ C$
Single pulse avalanche energy	E_{AS}	$L=0.1mH, V_{GS}=10V, R_g=25\Omega$,	-	282	mJ
		$L=0.5mH, V_{GS}=10V, R_g=25\Omega$,	-	680	mJ

ESD level (HBM)		CLASS 2
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● Thermal Resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}	-	-	1.2	°C/W
Thermal resistance, junction - ambient ^②	R_{thJA}	-	-	30	°C/W
Soldering temperature(total time<10s)	T_{sold}	-	-	260	°C

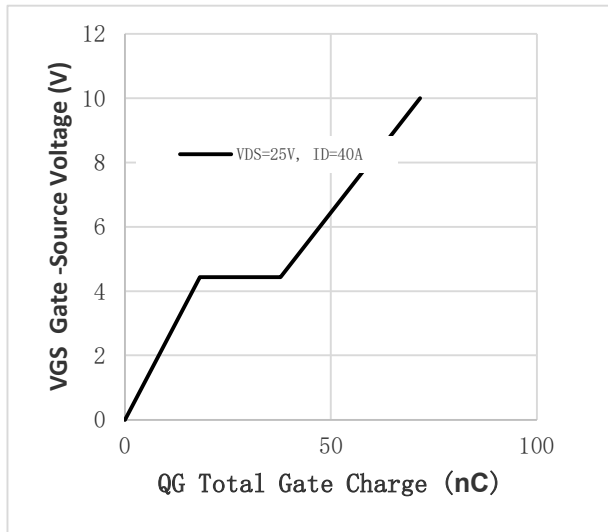
● Electronic Characteristics ($T_j=25^{\circ}\text{C}$, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2	2.7	3.5	V
Drain-source leakage current	I_{DSS}	$V_{GS}=0V, V_{DS}=40V$	-	-	1	μA
Gate- source leakage current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	100	nA
Static drain-source on resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=40A, T_j=25^{\circ}\text{C}$	-	1	1.3	m Ω
Forward transconductance	g_{FS}	$V_{DS}=5V, I_{SD}=10A$	-	30	-	S
Diode forward voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=40A$	-	-	1.3	V

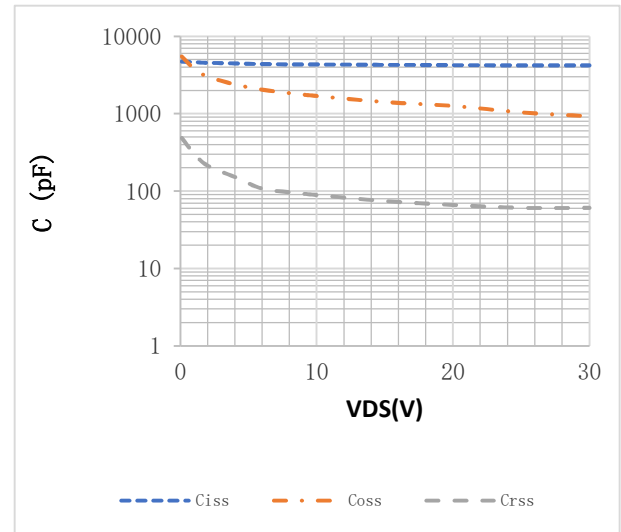
● Dynamic Characteristics ($T_j=25^{\circ}\text{C}$, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1\text{MHz}, V_{DS}=25V, V_{GS}=0V$	-	4220	-	pF
Output capacitance	C_{oss}		-	1160	-	pF
Reverse transfer capacitance	C_{rss}		-	61	-	pF
Gate resistance	R_g	$f=1\text{MHz}$	-	1.6	-	Ω
Total gate charge	Q_g	$V_{DD}=25V, I_D=40A, V_{GS}=10V$	-	71.6	-	nC
Gate-source charge	Q_{gs}		-	18.2	-	nC
Gate-drain charge	Q_{gd}		-	19.6	-	nC
Turn-on delay time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=15V, R_G=3.3\Omega, I_D=20A$	-	10	-	ns
Turn-on rise time	t_r		-	6	-	ns
Turn-off delay time	$t_{D(off)}$		-	25	-	ns
Turn-off fall time	t_f		-	15	-	ns
Reverse recovery time	t_{rr}	$V_{DD}=20V, dI_S/dt=100A/\mu s, I_S=50A$	-	59	-	ns
Reverse recovery charge	Q_{rr}		-	82	-	nC

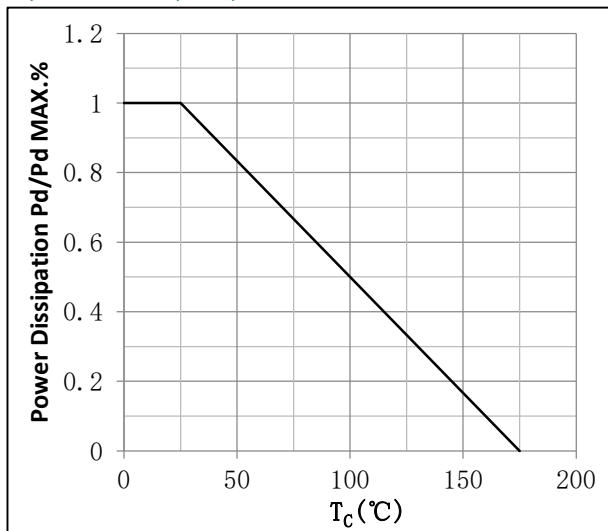
● Fig.1 Gate-source voltage as a function of gate charge; Typical values; $T_j=25^\circ\text{C}$



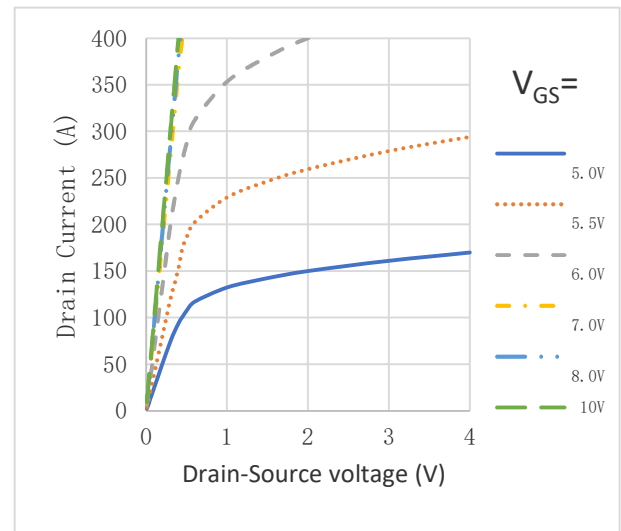
● Fig.2 Input, output and reverse transfer capacitances as a function of drain-source voltage; Typical values; $T_j=25^\circ\text{C}$



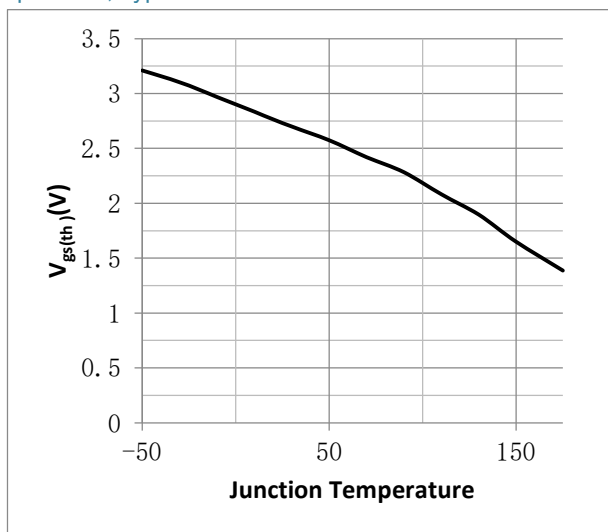
● Fig.3 Normalized total power dissipation as a function of case temperature; Calculative values Normalized Power Dissipation = $P_d/P_d(25^\circ\text{C})$



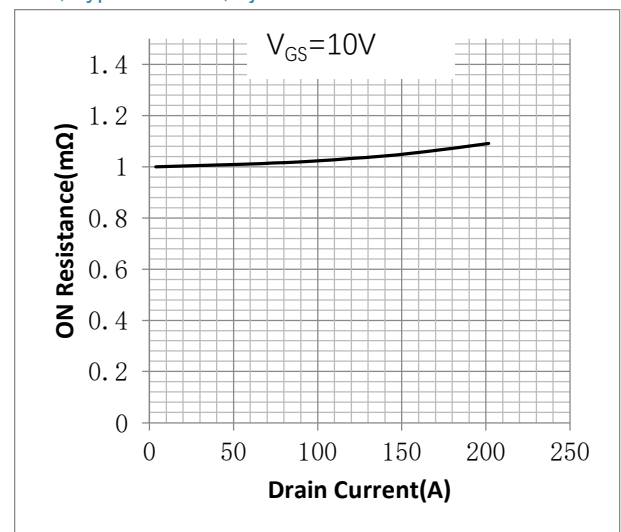
● Fig.4 Output characteristics: drain current as a function of drain-source voltage; Typical values; $T_j=25^\circ\text{C}$



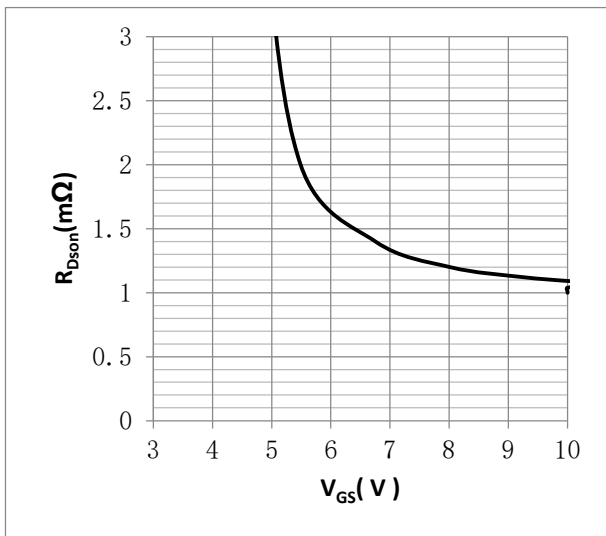
● Fig.5 Gate-source threshold voltage as a function of junction temperature; Typical values



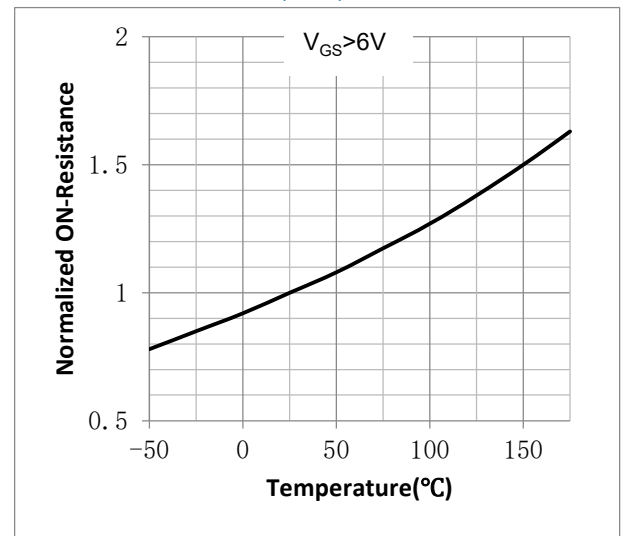
● Fig.6 Drain-source on-state resistance as a function of drain current; Typical values; $T_j=25^\circ\text{C}$



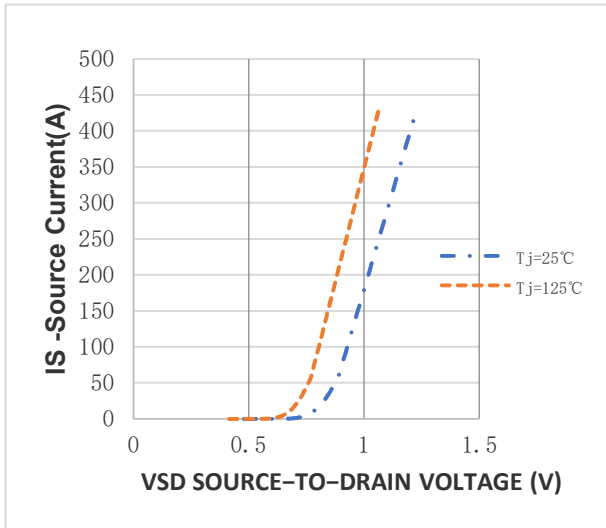
● Fig.7 Drain-source on-state resistance as a function of gate-source voltage; Typical values



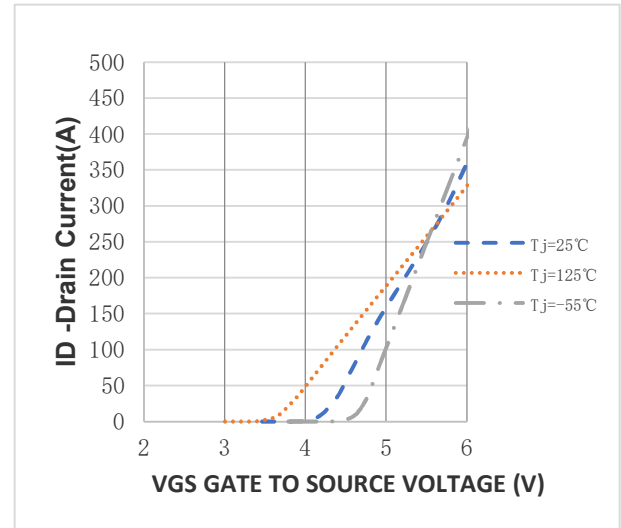
● Fig.8 Normalized drain-source on-state resistance factor as a function of junction temperature; Typical values Normalized On-Resistance=R_{DSon}/R_{DSon}(25°C)



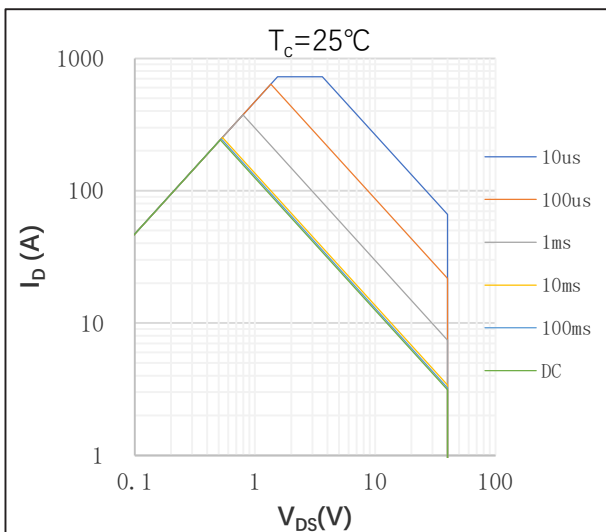
● Figure 9. Source (diode forward) current as a function of source-drain (diode forward) voltage; Typical values



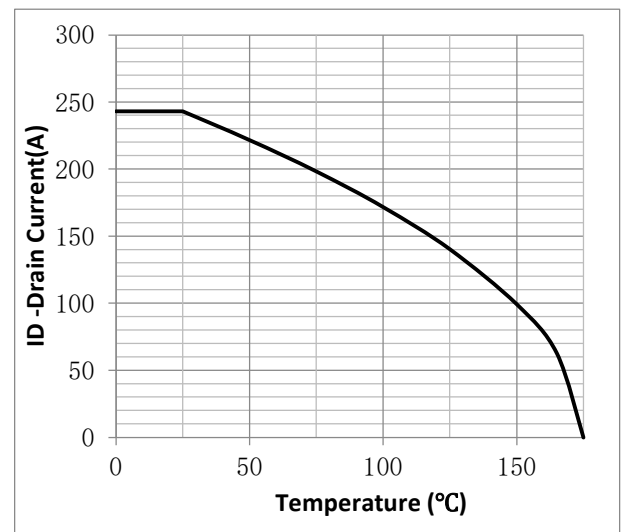
● Figure 10. Transfer characteristics: drain current as a function of gate-source voltage; Typical values



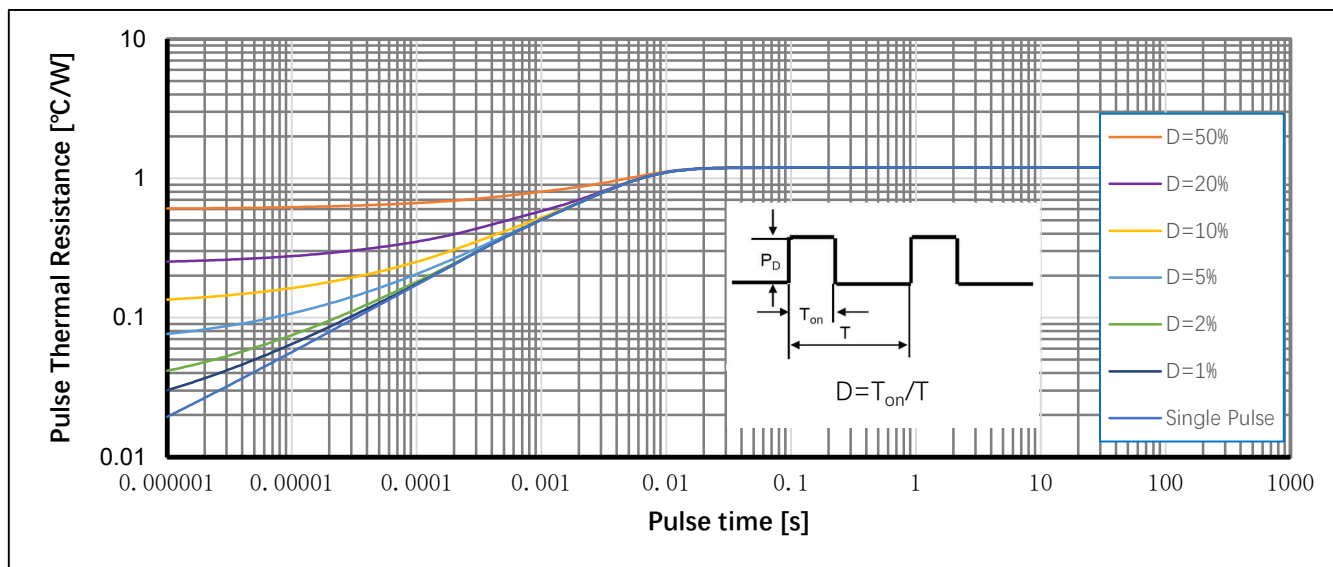
● Fig.11 Safe operating area: continuous and peak drain currents as a function of drain-source voltage; Calculative values



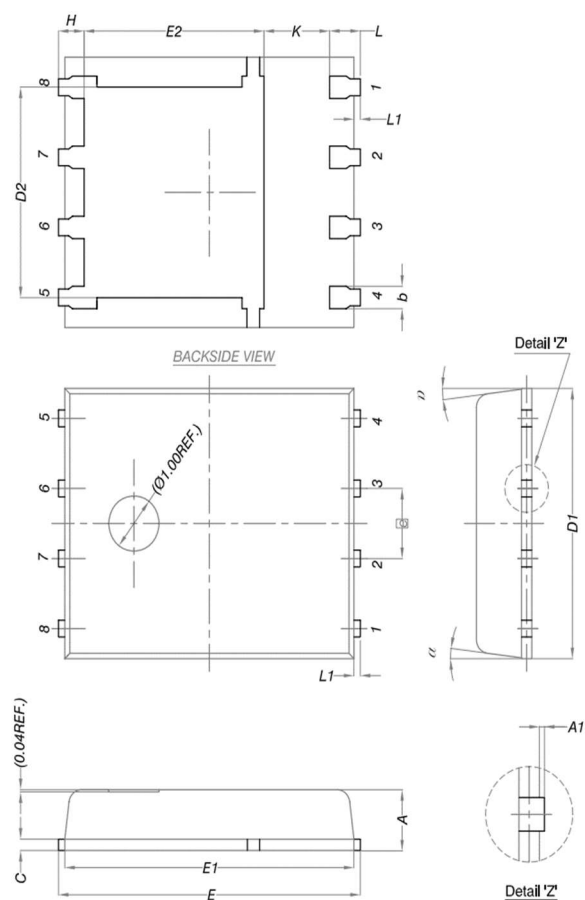
● Fig.12 Continuous drain current as a function of case temperature³; Calculative values



● Fig.13 Transient thermal impedance from junction to case as a function of pulse duration; max values



● Package Outline



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°

● Note

- ① Pulse : $V_{GS}=+20V/-20V$, Duty cycle=50%, $T_j=175^{\circ}C$, $t=1000$ hours; For DC , the following test conditions can be passed: $V_{GS}=+20V/-10V$, $T_j=175^{\circ}C$, $t=1000$ hours;
- ② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ③ Practically the current will be limited by PCB, thermal design and operating temperature. $V_{GS}=10V$.

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● Revision History

Version	Date	Change
A	2023/3/15	New
B	2023/6/25	Correct Rthjc
C	2023/12/18	Correct Package, Modify Rdson up limit, modify ID
C1	2025/4/3	Add body diode current
D	2025/12/15	1.Apply new datasheet format 2.Add transient thermal impedance curve. 3.Modify Qg,SOA. 4. Tighten VTH upper limit
E	2026/5/29	Modified ID